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Microprocessor for Image Down sampling

Design Documentation

# Design Description

This Processor design to down sample an image. The down sampling is done to obtain a 64\*64 pixel image from a 128\*128 grayscale image after applying 2\*2 Gaussian filtering.

# The Design

The C Program to down sample the image was written, then the C Program was then converted to assembly code, then the fallowing instruction set is derived.

## The ISA

The fallowing ISA is designed specifically for the image down sampling task and chose as the starting point for the design. The chart below elaborate their functionality.

|  |  |
| --- | --- |
| Instruction | Function |
| READ A | R 🡨 M[A] |
| WRITE B | M[B] 🡨 AC |
| JPNZ C | If Z== 0 PC 🡨 C , else PC 🡨 PC+2 |
| CLAC | AC 🡨 0 |
| ADD | AC 🡨 AC + R |
| SUB | AC 🡨 AC - R |
| R\_SHIFT | AC 🡨 AC << 1 |
| L\_SHIFT | AC 🡨 AC >> 1 |
| INC | AC 🡨 AC + 1 |

## The Micro Instructions

The following are the micro instructions used within the microprocessor and their description of operation.

|  |  |
| --- | --- |
| Micro Instruction | operation |
| FETCH 1 | AR 🡨 PC |
| FETCH 2 | DR 🡨 M[AR] , PC 🡨 PC+1 |
| FETCH 3 | IR 🡨 DR[3:0] , AR 🡨 PC |
| MEM 1 | DR 🡨 M[AR] , PC 🡨 PC+1 |
| MEM 2 | AR 🡨 PC , DR << 8 |
| MEM 3 | DR 🡨 M[AR] , PC 🡨 PC+1 |
| MEM 4 | AR 🡨 DR |
| READ 1 | DR 🡨 M[AR] |
| READ 2 | R 🡨 DR |
| WRITE 1 | M[AR] 🡨 AC |
| CLAC 1 | AC 🡨 0 Z 🡨 0 |
| ADD 1 | AC 🡨 AC + R , if (AC != 0) Z = 1 |
| SUB 1 | AC 🡨 AC - R , if (AC == 0) Z = 0 |
| R\_SHIFT 1 | AC 🡨 AC << 1 |
| L\_SHIFT 1 | AC 🡨 AC >> 1 |
| INC1 | AC 🡨 AC + 1 |
| JPNZ1 | PC 🡨 DR |
| JPNZ2 | PC 🡨 PC+1 |
| JPNZ3 | PC 🡨 PC+1 |

## Bus Architecture

ALUac

acALU

rALU

mdrr

mdrir

mdrpc

pcmar

mdrmar

acM

Mmdr

marM

AC

ALU

IR

PC

MDR

MAR

R

Memory

## State Diagram

## Signal Chart

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| STATE |  | Micro Instructions |  | PCINC | PCREAD | ACREAD | MARREADMDR | MARREADPC | MDRREAD | MDRSHIFT | RREAD | MEMWRITE | IRREAD | CLAC | ALUI |  | Control Signals |
| 1 |  | FETCH1 |  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 000 |  | 00001000000000 |
| 2 |  | FETCH2 |  | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 000 |  | 10000100000000 |
| 3 |  | FETCH3 |  | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 000 |  | 00001000010000 |
| 4 |  | MEM1 |  | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 000 |  | 10000100000000 |
| 5 |  | MEM2 |  | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 000 |  | 00001010000000 |
| 6 |  | MEM3 |  | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 000 |  | 10000100000000 |
| 7 |  | MEM4 |  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000 |  | 00010000000000 |
| 8 |  | READ1 |  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 000 |  | 00000100000000 |
| 9 |  | READ2 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 000 |  | 00000001000000 |
| 10 |  | WRITE1 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 000 |  | 00000000100000 |
| 11 |  | CLAC1 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 000 |  | 00000000001000 |
| 12 |  | ADD1 |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 001 |  | 00100000000001 |
| 13 |  | SUB1 |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 010 |  | 00100000000010 |
| 14 |  | R\_SHIFT1 |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 100 |  | 00100000000100 |
| 15 |  | L\_SHIFT1 |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 101 |  | 00100000000101 |
| 16 |  | INC1 |  | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 011 |  | 00100000000011 |
| 17 |  | JPNZ1 |  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000 |  | 01000000000000 |
| 18 |  | JPNZ2 |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000 |  | 10000000000000 |
| 19 |  | JPNZ3 |  | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 000 |  | 10000000000000 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  | Signal No |  | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2-0 |  |  |